

## Group No.

## Worksheet 9 EEL 4705

Emerging Logic Devices - K-Map based Mapping

(To convert AND/OR Logic to Majority Logic)



Question 1: Making use of the Algorithm and the K-Maps depicted, reduce the following function into a Majority Logic function. Each of the three functions  $(f_1, f_2, f_3)$  will be only from the Library of K-Map patterns depicted above.

- n = a.b.c + a.b.c + a.b.c + a.b.c
- Function needs to be broken in the form  $n = Maj(f_1, f_2, f_3)$ Find an admissible pattern for  $f_1$  from the above library.
- Find an admissible pattern for f<sub>1</sub> non the above notary.
   For finding f<sub>2</sub>, set Ψ<sub>1</sub> is obtained as follows: if a minterm of n is not a minterm of f<sub>1</sub>, add this minterm to Ψ<sub>1</sub>.
- Similarly, for finding  $f_2$ , set  $\Psi_0$  is obtained as follows: if a maxterm of n is not a maxterm of  $f_1$ , add this maxterm to  $\Psi_0$ .
- A suitable pattern for f₂ is then determined using new Ψ₁ and Ψ₀ (from the above library).
  Furthermore, to determine f₃, Ψ₁ and Ψ₀ are updated again as follows: if a minterm (maxterm) of node n is not a minterm (maxterm) of both f1 and f2, add this minterm (maxterm) to Ψ₁ (Ψ₀).



C





Ψ1



ΨO



C



Question 2: Perform the AND/OR mapping of the same expression n = a.b.c + a.b.c + a.b.c + a.b.c. Then see the difference in the number of majority gates used for K-map method and AND/OR method.



